

2007 Design, Automation & Test in Europe Conference & Exhibition

**Nice, France
16-20 April 2007**

Volume 1 of 3

**IEEE Catalog Number: 07EX1635
ISBN: 978-3-9810801-2-4**

Table of Contents

Keynote Addresses

Challenges of Digital Consumer and Mobile SOC's: More Moore Possible?	1
T. Furuyama	
Was Darwin Wrong? Has Design Evolution Stopped at the RTL Level... or Will Software and Custom Processors (or System-Level Design) Extend Moore's Law?	2
A. Naumann	

1.2: Design Records

Moderators: G. De Micheli, EPF Lausanne, CH, P. van der Wolf, NXP Semiconductors, NL

ATLAS: A Chip-Multiprocessor with Transactional Memory Support.....	3
N. Njoroge , J. Casper , S. Wee, Y. Teslyar, D. Ge, C. Kozyrakis and K. Olukotun	
A Dynamically Adaptive DSP for Heterogeneous Reconfigurable Platforms.....	9
F. Campi, A. Deledda, M. Pizzotti, L. Ciccarelli, P. Rolandi, C. Mucci, A. Lodi, A. Vitkovski and L. Vanzolini	
An 0.9 X 1.2", Low Power, Energy-Harvesting System with Custom Multi-Channel Communication Interface.....	15
P. Stanley-Marbell and D. Marculescu	

Interactive Presentation

An FPGA Based All-Digital Transmitter with Radio Frequency Output for Software Defined Radio	21
Z. Ye, J. Grosspietsch, G. Memik	

1.3 Design for Testability for SoCs

Moderators: S. Kundu, Massachusetts U, US, H.-J. Wunderlich, Stuttgart U, DE

A Non-Intrusive Isolation Approach for Soft Cores	27
O. Sinanoglu and T. Petrov	
Unknown Blocking Scheme for Low Control Data Volume and High Observability	33
S. Wang, W. Wei, S.T. Chakradhar	

Test Cost Reduction for SoC Using a Combined Approach to Test Data Compression and Test Scheduling.....	39
Q. Zhou and K.J. Balakrishnan	
High-Level Test Synthesis for Delay Fault Testability.....	45
S.-J. Wang and T.-H. Yeh	
1.4: Communication Synthesis under Timing Constraints	
<i>Moderators: J. Teich, Erlangen-Nuremberg U, DE, M. Heijligers, NXP Semiconductors, NL</i>	
Bus Access Optimisation for FlexRay-based Distributed Embedded Systems.....	51
T. Pop, P. Pop, P. Eles and Z. Peng	
A Decomposition-based Constraint Optimization Approach for Statically Scheduling Task Graphs with Communication Delays to Multiprocessors.....	57
N. Satish, K. Ravindran and K. Keutzer	
Design Closure Driven Delay Relaxation Based on Convex Cost Network Flow.....	63
C. Lin, A. Xie and H. Zhou	
1.5: Performance Modelling and Synthesis of Analogue/Mixed-Signal Circuits	
<i>Moderators: F. V. Fernandez, IMSE, CSIC and Seville U, ES, L. Hedrich, Frankfurt/M U, DE</i>	
Simulation-based Reusable Posynomial Models for MOS Transistor Parameters	69
V. Aggarwal and U.-M. O'Reilly	
Trade-Off Design of Analog Circuits Using Goal Attainment and “Wave Front” Sequential Quadratic Programming.....	75
D. Mueller, H. Graeb and U. Schlichtmann	
An Efficient Methodology for Hierarchical Synthesis of Mixed-Signal Systems with Fully Integrated Building Block Topology Selection.....	81
T. Eeckelaert, R. Schoofs, G. Gielen, M. Steyaert and W. Sansen	
Interactive Presentation	
A Coefficient Optimization and Architecture Selection Tool for $\Sigma\Delta$ Modulators in MATLAB	87
O. Yetik, O. Sağlamdemir, S. Talay and G. Dündar	
1.6: System Level Mapping and Simulation	
<i>Moderators: T. Henriksson, NXP Semiconductors, NL; L. Thiele, ETH Zurich, CH</i>	
Synthesis of Task and Message Activation Models in Real-Time Distributed Automotive Systems	93
W. Zheng, M. Di Natale, C. Pinello, P. Giusto and A. Sangiovanni Vincentelli	
An ILP Formulation for System-Level Application Mapping on Network Processor Architectures.....	99
C. Ostler and K.S. Chatha	
A Smooth Refinement Flow for Co-Designing HW and SW Threads.....	105
P. Destro, F. Fummi and G. Pravadelli	
Speeding Up SystemC Simulation through Process Splitting.....	111
Y. N. Naguib and R. S. Guindi	

Interactive Presentation

- An FPGA Design Flow for Reconfigurable Network-Based Multi-Processor Systems on Chip..... 117
A. Kumar, A. Hansson, J. Huisken and H. Corporaal

1.7: Algorithms and Applications of Run-Time Reconfiguration

Moderators: W. Najjar, UC Riverside, US, F. Kurdahi, UC Irvine, US

- Hard Real-Time Reconfiguration Port Scheduling 123
F. Dittmann and S. Frank
- An Efficient Algorithm for Online Management of 2D Area of Partially Reconfigurable FPGAs 129
J. Cui, Q. Deng, X. He and Z. Gu
- Improving Utilization of Reconfigurable Resources Using Two-Dimensional Compaction..... 135
A.A. El Farag, H.M. El-Boghdadi and S.I. Shaheen
- Low-Power Warp Processor for Power Efficient High-Performance Embedded Systems 141
R. Lysecky

Interactive Presentations

- Using Dynamic Voltage Scaling to Reduce the Configuration Energy of Run Time Reconfigurable
Devices..... 147
Y. Qu, J.-P. Soininen and J. Nurmi
- A Shift Register Based Clause Evaluator for Reconfigurable SAT Solver..... 153
M. Safar, M. Shalan, M. W. El-Kharashi and A. Salem

2.2 IP Designs for Media Processing and Other Computational Intensive Kernels

Moderators: J. Dielissen, NXP Semiconductors, NL, N. Dutt, UC Irvine, US

- Efficient High-Performance ASIC Implementation of JPEG-LS Encoder 159
M. Papadonikolakis, V. Pantazis and A. P. Kakarountas
- Improve CAM Power Efficiency Using Decoupled Match Line Scheme..... 165
Y.-J. Chang, Y.-H. Liao and S.-J. Ruan
- Cyclostationary Feature Detection on a Tiled-SoC..... 171
A. B. J. Kokkeler, G. J. M. Smit, T. Krol and J. Kuper
- Mapping Control-Intensive Video Kernels onto a Coarse-Grain Reconfigurable Architecture:
The H.264/AVC Deblocking Filter 177
C. Arbelo, A. Kanstein, S. López, J. F. López, M. Berekovic, R. Sarmiento and J.-Y. Mignolet

Interactive Presentations

- An Efficient Hardware Architecture for H.264 Intra Prediction Algorithm 183
E. Sahin and I. Hamzaoglu
- An FPGA Implementation of Decision Tree Classification..... 189
R. Narayanan, D. Honbo, G. Memik, A. Choudhary and J. Zambreno
- Radix 4 SRT Division with Quotient Prediction and Operand Scaling 195
N.R. Srivastava

2.3: Test Infrastructure of SoCs and its Verification

Moderators: F. Novak, Jozef Stefan Institute, SL, R. Dorsch, IBM, Boeblingen, DE

SoC Testing Using LFSR Reseeding, and Scan-Slice-Based TAM Optimization and Test Scheduling	201
Z. Wang, K. Chakrabarty and S. Wang	
Optimized Integration of Test Compression and Sharing for SoC Testing.....	207
A. Larsson, E. Larsson, P. Eles and Z. Peng	
A Sophisticated Memory Test Engine for LCD Display Drivers.....	213
O. Spang, H.-M. von Staudt and M.G. Wahl	
Formal Verification of a Pervasive Interconnect Bus System in a High-Performance Microprocessor	219
T. Le, T. Glöckler and J. Baumgartner	

Interactive Presentations

Low Cost Debug Architecture Using Lossy Compression for Silicon Debug	225
E. Anis and N. Nicolici	
An SoC Test Scheduling Algorithm Using Reconfigurable Union Wrappers	231
T. Yoneda, M. Imanishi and H. Fujiwara	

2.4: HOT TOPIC – Microprocessors in the Era of Terascale Integration

Moderator: A. González, Intel and UPC, ES

Microprocessors in the Era of Terascale Integration.....	237
S. Borkar, N.P. Jouppi and P. Stenstrom	

2.5: Statistical / Nonlinear Analysis and Verification for Analogue Circuits

Moderators: G. Vandersteen, IMEC, BE, J. Roychowdhury, Minnesota U, US

CMCal: An Accurate Analytical Approach for the Analysis of Process Variations with Non-Gaussian Parameters and Nonlinear Functions.....	243
M. Zhang, M. Olbrich, D. Seider, M. Frerichs, H. Kinzelbach and E. Barke	
A Symbolic Methodology for the Verification of Analog and Mixed Signal Designs	249
G. Al-Sammam, M. H. Zaki and S. Tahar	
Efficient Nonlinear Distortion Analysis of RF Circuits	255
D. Tannir and R. Khazaka	
Nonlinearity Analysis of Analog/RF Circuits Using Combined Multisine and Volterra Analysis.....	261
J. Borremans, L. De Locht, P. Wambacq and Y. Rolain	

Interactive Presentation

Optimizing Analog Filter Designs for Minimum Nonlinear Distortions Using Multisine Excitations.....	267
J. Lataire, G. Vandersteen and R. Pintelon	

2.6: System Modeling and Specification

Moderators: T. Schattkowsky, Paderborn U, DE, W. Klingauf, TU Braunschweig, DE

Performance Analysis of Complex Systems by Integration of Dataflow Graphs and Compositional Performance Analysis.....	273
S. Schliecker, S. Stein and R. Ernst	

Tackling an Abstraction Gap: Co-Simulating with SystemC DE and Bluespec ESL	279
H.D. Patel and S.K Shukla	
A Calculator for Pareto Points	285
M. Geilen and T. Basten	
Modeling and Simulation to the Design of $\Sigma\Delta$ Fractional-N Frequency Synthesizer	291
S. Huang, H. Ma and Z. Wang	
Interactive Presentations	
System Level Power Optimization of Sigma-Delta Modulator	297
F. Gong and X. Wu	
Executable System-Level Specification Models Containing UML-Based Behavioral Patterns	301
L.S. Indrusiak, A. Thuy and M. Glesner	
2.7: Design Space Exploration and Nano-Technologies for Reconfigurable Computing	
<i>Moderators: W. Luk, Imperial College, London, UK, R. Lysecky, Arizona U, US</i>	
Assessing Carbon Nanotube Bundle Interconnect for Future FPGA Architectures.....	307
S. Eachempati, A. Nieuwoudt, A. Gayasen, N. Vijaykrishnan and Y. Massoud	
Two-Level Microprocessor-Accelerator Partitioning	313
S. Sirowy, Y. Wu, S. Lonardi and F. Vahid	
Design Space Exploration of Partially Re-Configurable Embedded Processors.....	319
A. Chattopadhyay, W. Ahmed, K. Karuri, D. Kammler, R. Leupers, G. Ascheid and H. Meyr	
Interactive Presentation	
Generating and Executing Multi-Exit Custom Instructions for an Adaptive Extensible Processor	325
H. Noori, F. Mehdipour, K. Murakami, K. Inoue and M. Goudarzi	
3.2: Implementation of LDPC Codecs for Various Communication Standards	
<i>Moderators: M. Heijligers, NXP Semiconductors, NL, N. Wehn, Kaiserslautern U, DE</i>	
Low Complexity LDPC Code Decoders for Next Generation Standards	331
T. Brack, M. Alles, T. Lehnigk-Emden, F. Kienle, N. Wehn, N.E. L'Insalata, F. Rossi, M. Rovini and L. Fanucci	
Non-Fractional Parallelism in LDPC Decoder Implementations	337
J. Dielissen and A. Hekstra	
Minimum-Energy LDPC Decoder for Real-Time Mobile Application	343
W. Wang and G. Choi	
Pipelined Implementation of a Real Time Programmable Encoder for Low Density Parity Check Code on a Reconfigurable Instruction Cell Architecture	349
Z. Khan and T. Arslan	
Interactive Presentation	
Implementation of AES/Rijndael on a Dynamically Reconfigurable Architecture	355
C. Mucci, L. Vanzolini, A. Lodi, A. Deledda, R. Guerrieri, F. Campi and M. Toma	

3.3: Testing NoCs

Moderators: Z. Peng, Linköping U, SE; J. Raik, TU Tallinn, ES

Using the Inter- and Intra-Switch Regularity in NoC Switch Testing	361
M. Hosseinabady, A. Dalirsani and Z. Navabi	
Toward a Scalable Test Methodology for 2D-Mesh Network-on-Chips.....	367
K. Petersén and J. Öberg	
Remote Testing and Diagnosis of System-on-Chips Using Network Management Frameworks.....	373
O. Laouamri and C. Aktouf	

3.4: Synthesis at System and Architectural Levels

Moderators: P. Pop, DTU, DK; S. Chakraborty, National U of Singapore, SG

Fast Memory Footprint Estimation Based on Maximal Dependency Vector Calculation	379
Q. Hu, A. Vandecappelle, P.G. Kjeldsberg, F. Catthoor and M. Palkovic	
Mapping Multi-Dimensional Signals into Hierarchical Memory Organizations	385
H. Zhu, I.I. Lucian and F. Balasa	
The Impact of Loop Unrolling on Controller Delay in High Level Synthesis	391
S. Kurra, N.K. Singh and P.R. Panda	
Clock-Frequency Assignment for Multiple Clock Domain Systems-on-a-Chip.....	397
S. Sirowy, Y. Wu, S. Lonardi and F. Vahid	

Interactive Presentations

System-Level Process Variation Driven Throughput Analysis for Single and Multiple Voltage-Frequency Island Designs	403
S. Garg and D. Marculescu	
Reliability-Aware System Synthesis.....	409
M. Glass, M. Lukasiewicz, T. Streichert, C. Haubelt and J. Teich	

3.5: Analogue and Mixed-Signal Design and Characterization

Moderators: A. Rodriguez-Vazquez, AnaFocus, ES; M. Glesner, TU Darmstadt, DE

Flexibility-Oriented Design Methodology for Reconfigurable Delta Sigma Modulators.....	415
P. Sun, Y. Wei and A. Dobil	
Experimental Validation of a Tuning Algorithm for High-Speed Filters.....	421
G. Matarrese, C. Marzocca, F. Corsi, S. D'Amico and A. Baschiroto	
Design of High-Resolution MOSFET-Only Pipelined ADCs with Digital Calibration.....	427
H. Aminzadeh, M. Danaie and R. Lotfi	
A New Technique for Characterization of Digital-to-Analog Converters in High-Speed Systems	433
J. Savoj, A.-A. Abbasfar, A. Amirkhany, B. W. Garlepp and M. A. Horowitz	

3.6: PANEL SESSION – Should You Trust the Surgeon or the Family Doctor?

Organizer: M. Casale-Rossi, Synopsys, Italy

Moderator: A. Strojwas, Carnegie Mellon U, US

DFM/DFY: Should You Trust the Surgeon or the Family Doctor?	439
Panelists: R. Aitken, A. Domic, C. Guardiani, P. Magarshack, D. Pattullo, J. Sawicki	

3.7: Automatic Synthesis of Computation Intensive Application Specific Circuits

Moderators: F. Ferrandi, Politecnico di Milano, IT; T. Henriksson, NXP Semiconductors, NL

Automatic Synthesis of Compressor Trees: Reevaluating Large Counters.....	443
A.K. Verma and P. Ienee	

Area Optimization of Multi-Cycle Operators in High-Level Synthesis.....	449
M.C. Molina, R. Ruiz-Sautua, J.M. Mendias and R. Hermida	

Data-Flow Transformations Using Taylor Expansion Diagrams	455
M. Ciesielski, S. Askar, D. Gomez-Prado, J. Guillot and E. Boutillon	

Automatic Application Specific Floating-Point Unit Generation.....	461
Y.J. Chong and S. Parameswaran	

Interactive Presentation

Time-Constrained Clustering for DSE of Clustered VLIW-ASP	467
M. Schölzel	

4.1: EMBEDDED TUTORIAL – Applications for Ubiquitous Computing and Communications (Ubiquitous Communication and Computation Special Day)

Organizer/Moderator: P Liuha, Nokia, FI

Applications for Ubiquitous Computing and Communications	473
--	-----

4.2: Automotive

Moderators: L. Fanucci, Pisa U, IT; J. Gerlach, Robert Bosch GmbH, DE

Timing Simulation of Interconnected AUTOSAR Software-Components	474
M. Krause, O. Bringmann, A. Hergenhan, G. Tabanoglu and W. Rosenstiel	

FPGA-Based Networking Systems for High Data-Rate and Reliable In-Vehicle Communications.....	480
S. Saponara, E. Petri, M. Tonarelli, I. Del Corona and L. Fanucci	

Low-g Accelerometer Fast Prototyping for Automotive Applications	486
F. D’Ascoli, F. Iozzi, C. Marino, M. Melani, M. Tonarelli, L. Fanucci, A. Giambastiani, A. Rocchi and M. De Marinis	

Using an Innovative SOC-Level FMEA Methodology to Design in Compliance with IEC61508.....	492
R. Mariani, G. Boschi and F. Colucci	

Using Partial-Run-Time Reconfigurable Hardware to Accelerate Video Processing in Driver Assistance Systems.....	498
C. Claus, J. Zeppenfeld, F. Müller and W. Stechele	

Interactive Presentation

Towards a Methodology for the Quantitative Evaluation of Automotive Architectures	504
P. Popp, M. Di Natale, P. Giusto, S. Kanajan and C. Pinello	

4.3: Test Generation for Diagnosis, Scan Testing and Advanced Memory Fault Models

Moderators: H. Obermeir, Infineon Technologies AG, DE; B. Straube, FhG IIS/EAS Dresden, DE

Dynamic Learning Based Scan Chain Diagnosis.....	510
Y. Huang	
Diagnosis, Modeling and Tolerance of Scan Chain Hold-Time Violations.....	516
O. Sinanoglu and P. Schremmer	
On Test Generation by Input Cube Avoidance	522
I. Pomeranz and S.M. Reddy	
Slow Write Driver Faults in 65nm SRAM Technology: Analysis and March Test Solution.....	528
A. Ney, P. Girard, C. Landrault, S. Pravossoudovitch, A. Virazel and M. Bastian	

Interactive Presentations

On Power-Profiling and Pattern Generation for Power-Safe Scan Tests.....	534
V.R. Devanathan, C.P. Ravikumar and V. Kamakoti	
Automatic Test Pattern Generation for Maximal Circuit Noise in Multiple Aggressor Crosstalk Faults.....	540
K.P. Ganeshpure and S. Kundu	

4.4: Future Design Challenges

Moderators: V. Narayanan, Penn State U, US; C. Guiducci, Bologna U, IT

Temperature-Aware NBTI Modeling and the Impact of Input Vector Control on Performance Degradation.....	546
Y. Wang, H. Luo, K. He, R. Luo, H. Yang and Y. Xie	
A Cross-Referencing-Based Droplet Manipulation Method for High-Throughput and Pin-Constrained Digital Microfluidic Arrays.....	552
T. Xu and K. Chakrabarty	
Reversible Circuit Technology Mapping from Non-Reversible Specifications	558
Z. Zilic, K. Radecka and A. Khazamiphur	
Distributed Power-Management Techniques for Wireless Network Video Systems.....	564
N. H. Zamora, J.-C. Kao and R. Marculescu	

Interactive Presentations

Improving the Fault Tolerance of Nanometric PLA Designs	570
F. Angiolini, M.H. Ben Jamaa, D. Atienza, L. Benini, and G. De Micheli	
Techniques for Designing Noise-Tolerant Multi-Level Combinational Circuits.....	576
K. Nepal, R.I. Bahar, J. Mundy, W.R. Patterson and A. Zaslavsky	

4.5: Application-Specific Architectures

Moderators: T. Austin, U of Michigan, US; B. Calder, Microsoft, US

An Efficient Code Compression Technique Using Application-Aware Bitmask and Dictionary Selection Methods.....	582
S.-W. Seong and P. Mishra	
Optimizing Instruction-Set Extensible Processors under Data Bandwidth Constraints.....	588
K. Atasu, R.G. Dimond, O. Mencer, W. Luk, C. Özturan and G. Dündar	
Resource Prediction for Media Stream Decoding.....	594
J. Hamers and L. Eeckhout	
Register Pointer Architecture for Efficient Embedded Processors	600
J.S. Park, S.-B. Park, J.D. Balfour, D. Black-Schaffer, C. Kozyrakis and W.J. Dally	

Interactive Presentations

Feasibility of Combined Area and Performance Optimization for Superscalar Processors Using Random Search	606
S. Van Haastregt and P.M.W. Knijnenburg	
A Decoupled Architecture of Processors with Scratch-Pad Memory Hierarchy	612
A. Milidonis, N. Alachiotis, V. Porpodas, H. Michail, A.P. Kakarountas and C.E. Goutis	

4.6: Technology and Process Aware Low Power Circuit Design

Moderators: A.J. Acosta, Seville U/IMSE, ES; B.C. Paul, Toshiba, US

An Algorithm to Minimize Leakage through Simultaneous Input Vector Control and Circuit Modification	618
N. Jayakumar and S.P. Khatri	
Understanding Voltage Variations in Chip Multiprocessors Using a Distributed Power-Delivery Network	624
M.S. Gupta, J.L. Oatley, R. Joseph, G.-Y. Wei and D.M. Brooks	
Process Variation Tolerant Low Power DCT Architecture.....	630
N. Banerjee, G. Karakonstantis and K. Roy	

Interactive Presentation

Statistical Dual-Vdd Assignment for FPGA Interconnect Power Reduction.....	636
Y. Lin and L. He	

4.7: Hardware Implementation of MPSoCs and NoCs Architectures

Moderators: K. Goossens, NXP Semiconductors, NL; B. Candaele, Thales Communications, FR

Hardware Scheduling Support in SMP Architectures	642
A.C. Nácul, F. Regazzoni and M. Lajolo	
A Scalable, Timing-Safe, Network-on-Chip Architecture with an Integrated Clock Distribution Method	648
T. Bjerregaard, M.B. Stensgaard and J. Sparsø	
Butterfly and Benes-Based On-Chip Communication Networks for Multiprocessor Turbo Decoding.....	654
H. Moussa, O. Muller, A. Baghdadi and M. Jézéquel	

Interactive Presentation

Capturing the Interaction of the Communication, Memory and I/O Subsystems in Memory-Centric Industrial MPSoC Platforms	660
S. Medardoni, M. Ruggiero, D. Bertozzi, L. Benini, G. Strano and C. Pistrutto	

5.1.1: HOT TOPIC I: Security and Trust in Ubiquitous Communication (Ubiquitous Communication and Computation Special Day)

Organizer/Moderator: P. Liuha, Nokia, FI

Cost-Aware Capacity Optimization in Dynamic Multi-Hop WSNs	666
J. Suhonen, M. Kohvakka, M. Kuorilehto, M. Hännikäinen, and T.D. Hämäläinen	
Design Methods for Security and Trust	672
I. Verbauwhede and P. Schaumont	

5.1.2: Lunch-Time Keynote (Ubiquitous Communication and Computation Special Day)

Emerging Solutions Technology and Business Views for the Ubiquitous Communication	678
H. Huomo	

5.2: Industrial System Designs in Aerospace, Avionics and Automotive

Moderators: L. Fanucci, Pisa U, IT; A. Reutter, Robert Bosch GmbH, DE

Development of on Board, Highly Flexible, Galileo Signal Generator ASIC	679
L. Baguena, E. Liégeon, A. Bépoix, J.-M. Dusserre, C. Oustric, P. Bellocq and V. Heiries	
New Safety Critical Radio Altimeter for Airbus and Related Design Flow.....	684
D. Hairion, S. Emeriau, E. Combot and M. Sarlotte	
Introducing New Verification Methods into a Company's Design Flow: An Industrial User's Point of View	689
R. Lissel and J. Gerlach	

5.3: Mixed-Signal and RF Test

Moderators: A. Chatterjee, Georgia Institute of Technology, US; B. Kaminska, Simon Fraser U, CA

Testable Design for Advanced Serial-Link Transceivers.....	695
M. Lin and K.-T. Cheng	
Method for Reducing Jitter in Multi-Gigahertz ATE.....	701
D.C. Keezer, D. Minier and P. Ducharme	
Re-Configuration of Sub-Blocks for Effective Application of Time Domain Tests.....	707
J. Anders, S. Krishnan and G. Gronthoud	
An ADC-BiST Scheme Using Sequential Code Analysis	713
E.S. Erdogan and S. Ozev	

Interactive Presentation

Boosting SER Test for RF Transceivers by Simple DSP Technique	719
J. Dabrowski and R. Ramzan	
Novel Test Infrastructure and Methodology Used for Accelerated Bring-Up and In-System Characterization of the Multi-Gigahertz Interfaces on the Cell Processor.....	725
P. Yeung, A. Torres and P. Batra	

Evaluation of Test Measures for LNA Production Testing Using a Multinormal Statistical Model.....	731
J. Tongbong, S. Mir and J.L. Carbonero	

5.4: EMBEDDED TUTORIAL AND PANEL – Heterogeneous Systems on Chip and Systems in Package

Organizers/Moderators: B. Courtois, TIMA Laboratory, FR; I. O'Connor, Ecole Centrale de Lyon, FR

Heterogeneous Systems on Chip and Systems in Package	737
I. O'Connor, B. Courtois, K. Chakrabarty, N. Delorme, M. Hampton, J. Hartung	

5.5: Novel Directions in Architectural Simulation and Validation

Moderators: E.M. Aboulhamid, Montreal U, CA; T. Austin, U of Michigan, US

Engineering Trust with Semantic Guardians	743
I. Wagner and V. Bertacco	

CATS: Cycle Accurate Transaction-Driven Simulation with Multiple Processor Simulators.....	749
D. Kim, S. Ha and R. Gupta	

A One-Shot Configurable-Cache Tuner for Improved Energy and Performance	755
A. Gordon-Ross, P. Viana, F. Vahid, W. Najjar and E. Barros	

Design Fault Directed Test Generation for Microprocessor Validation.....	761
D.A. Mathaikutty, S.K. Shukla, S.V. Kodakara, D. Lilja and A. Dingankar	

Interactive Presentation

Impact of Description Language, Abstraction Layer, and Value Representation on Simulation Performance.....	767
W. Ecker, V. Esen, L. Schönberg, T. Steininger M. Velten and M. Hull	

5.6: Power Management

Moderators: D. Soudris, Thrace Democritus U, GR; M. Poncino, Politecnico di Torino, IT

Adaptive Power Management in Energy Harvesting Systems.....	773
C. Moser, L. Thiele, D. Brunelli and L. Benini	

Stochastic Modeling and Optimization for Robust Power Management in a Partially Observable System.....	779
Q. Qiu, Y. Tan and Q. Wu	

Efficient and Scalable Compiler-Directed Energy Optimization for Realtime Applications.....	785
P.-K. Huang and S. Ghiasi	

Interactive Presentations

Peripheral-Conscious Scheduling on Energy Minimization for Weakly Hard Real-Time Systems.....	791
L. Niu and G. Quan	

Task Scheduling under Performance Constraints for Reducing the Energy Consumption of GALS Multi-Processor SoC.....	797
R. Watanabe, M. Kondo, M. Imai, H. Nakamura and T. Nanya	

5.7: Advanced Techniques for Embedded Processors Design

Moderators: W. Kruijtzter, NXP Semiconductors, NL; G. Martin, Tensilica, US

Instruction Trace Compression for Rapid Instruction Cache Simulation.....	803
A. Janapsatya, A. Ignjatovic, S. Parameswaran and J. Henkel	
Efficient Code Density through Look-Up Table Compression.....	809
T. Bonny and J. Henkel	
Microarchitectural Support for Program Code Integrity Monitoring in Application-Specific Instruction Set Processors	815
Y. Fei and Z.J. Shi	

Interactive Presentation

Soft-Core Processor Customization Using the Design of Experiments Paradigm.....	821
D. Sheldon, F. Vahid and S. Lonardi	

6.1: HOT TOPIC II: Power Supply and Power Management in UbiCom (Ubiquitous Communication and Computation Special Day)

Power Supply and Power Management in UbiCom.....	827
--	-----

6.2: Best Industrial Systems Designs in Communication and Multimedia

Moderators: O. Deprez, Texas Instruments, FR; M. Heijligers, NXP Semiconductors, NL

From Algorithm to First 3.5G Call in Record Time – A Novel System Design Approach Based on Virtual Prototyping and Its Consequences for Interdisciplinary System Design Teams.....	828
M. Brandenburg, A. Schöllhom, S. Heinen, J. Eckmüller and T. Eckart	
Portable Multimedia SoC Design: A Global Challenge.....	831
M. Paganini, G. Kimmich, S. Ducrey, G. Caubit and V. Coeffe	
What If You Could Design Tomorrow’s System Today?	835
N. Wingen	

6.3: Nano and FIFO

Moderators: E. Larsson, Linköping U, SE; D. Gizopoulos, Piraeus U, GR

Circuit-Level Modeling and Detection of Metallic Carbon Nanotube Defects in Carbon Nanotube FETs.....	841
H. Hashempour and F. Lombardi	
Error Rate Reduction in DNA Self-Assembly by Non-Constant Monomer Concentrations and Profiling	847
B. Jang, Y.-B. Kim and F. Lombardi	
Design and DFT of a High-Speed Area-Efficient Embedded Asynchronous FIFO.....	853
P. Wielage, E.J. Marinissen, M. Altheimer and C. Wouters	
Test Quality Analysis and Improvement for an Embedded Asynchronous FIFO.....	859
T. Dubois, M. Azimane, E. Larsson, E.J. Marinissen, P. Wielage and C. Wouters	

Interactive Presentation

Logic Level Fault Tolerance Approaches Targeting Nanoelectronics PLAs.....	865
W. Rao, A. Orailoglu and R. Karri	

6.4: System Level Validation

Moderators: F. Fummi, Verona U, IT; M. Lajolo, NEC Laboratories, US

A Multi-Core Debug Platform for NoC-Based Systems	870
S. Tang and Q. Xu	
Seamless Hardware/Software Performance Co-Monitoring in a Codesign Simulation Environment with RTOS Support.....	876
L. Moss, M. de Nanclas, L. Filion, S. Fontaine, G. Bois and M. Aboulhamid	
Incremental ABV for Functional Validation of TL-to-RTL Design Refinement.....	882
N. Bombieri, F. Fummi and G. Pravadelli	
Efficient Testbench Code Synthesis for a Hardware Emulator System	888
I. Mavroidis and I. Papaefstathiou	

Interactive Presentations

Implementation of a Transaction Level Assertion Framework in SystemC.....	894
W. Ecker, V. Esen, T. Steininger, M. Velten and M. Hull	
Automatic Generation of Functional Coverage Models from Behavioral Verilog Descriptions	900
S. Verma, I.G. Harris and K. Ramineni	

6.5: Model-Based Design for Embedded Systems

Moderators: P.J. Mosterman, The MathWorks, Inc, US; H. Giese, Paderborn U, DE

Compositional Specification of Behavioral Semantics	906
K. Chen, J. Sztipanovits and S. Neema	
Performance Analysis of Multimedia Applications Using Correlated Streams	912
K. Huang, L. Thiele, T. Stefanov and E. Deprettere	
Simulation Platform for UHF RFID	918
V. Derbek, C. Steger, R. Weiß, D. Wischounig, J. Preishuber-Pfluegl and M. Pistauer	
Tool-Support for the Analysis of Hybrid Systems and Models	924
A. Bauer, M. Pister and M. Tautschnig	

Interactive Presentation

Automatic Model Generation for Black Box Real-Time Systems	930
T.H. Feng, L. Wang, W. Zheng, S. Kanajan and S.A. Seshia	

6.6: PANEL SESSION – Life Begins at 65 – Unless You Are Mixed Signal

Organizers: N. Nandra, Synopsys, US; R. Wittmann, Nokia, DE

Moderator: G. Gielen, KU Leuven, BE

Life Begins at 65 – Unless You Are Mixed Signal?	936
R. Wittmann, N. Nandra, J. Kunkel, M. Vanzi, J. Franca, H.-J. Wassener, C. Münker	

6.7: Resource Optimisation for Best Effort and Quality of Service

Moderators: M. Coppolla, STMicroelectronics, IT; P. Ienne, EPFL Lausanne, CH

Routing Table Minimization for Irregular Mesh NoCs.....	942
E. Bolotin, I. Cidon, R. Ginosar and A. Kolodny	

Congestion-Controlled Best-Effort Communication for Networks-on-Chip 948
J.W. van den Brand, C. Ciordas, K. Goossens and T. Basten

Undisrupted Quality-of-Service during Reconfiguration of Multiple Applications in Networks on Chip 954
A. Hansson, M. Coenen and K. Goossens

7.1 HOT TOPIC – Testing 35 Billions of Transistors in 2020, Is It Possible?

*Organizers: L. Anghel, TIMA Laboratory, FR; M.-L. Flottes, LIRMM, Montpellier, FR
Moderator Y. Zorian, Virage Logic, US*

Testing in the Year 2020 960
R. Galivanche, R. Kapur and A. Rubio

7.2 Designs in Avionics, Military and Space

Moderators: P. Manet, U Catholique de Louvain, BE ; I. Soderquist, SAAB AB, Saab Avitronics, SE

Transaction Level Modeling of SCA Compliant Software Defined Radio Waveforms and
Platforms PIM/PSM 966
G. Gailliard, E. Nicollet, M. Sarlotte and F. Verdier

Event Driven Data Processing Architecture 972
I. Söderquist

Reconfigurable System-on-Chip Data Processing Units for Space Imaging Instruments 977
B. Fiethe, H. Michalik, C. Dierker, B. Osterloh and G. Zhou

Enabling Certification for Dynamic Partial Reconfiguration Using a Minimal Flow 983
B. Rousseau, P. Manet, D. Galerin, D. Merkenbraeck, J.-D. Legat , F. Dedeken and Y. Gabriel

Identification of Process/Design Issues during 0.18 μm Technology Qualification for
Space Application 989
J. Ferrigno, P. Perdu, K. Sanchez and D. Lewis

Interactive Presentations

RECOPS: Reconfiguring Programmable Devices for Military Hardware Electronics 994
P. Manet, D. Maufroid, L. Tosi, M. Di Ciano, O. Mulertt, Y. Gabriel, J.-D. Legat, D. Aulagnier,
C. Gamrat, R. Liberati and V. La Barba

7.4: Timing Analysis and Validation

Moderators: F. Salice, Politecnico di Milano, IT; P. Sanchez, Cantabria U, ES

WAVSTAN: Waveform Based Variational Static Timing Analysis 1000
S.K Tiwary and J.R. Phillips

Rapid and Accurate Latch Characterization via Direct Newton Solution of Setup/Hold Times 1006
S. Srivastava and J. Roychowdhury

Temperature and Voltage Aware Timing Analysis: Application to Voltage Drops 1012
B. Lasbouygues, R. Wilson, N. Azemard and P. Maurine

Accurate Timing Analysis Using SAT and Pattern-Dependent Delay Models 1018
D. Tadesse, D. Sheffield, E. Lenge, R.I. Bahar and J. Grodstein

7.5: Model-Based Analysis and Middleware of Embedded Systems

Moderators: S. van Loo, Philips Research, NL; H. De Groot, European Microsoft Innovation Centre, DE

CARAT: A Toolkit for Design and Performance Analysis of Component-Based Embedded Systems.....	1024
E. Bondarev, M. Chaudron and P.H.N. de With	
Modeling and Simulation Alternatives for the Design of Networked Embedded Systems.....	1030
E. Alessio, F. Fummi, D. Quaglia and M. Turolla	
Middleware Design Optimization of Wireless Protocols Based on the Exploitation of Dynamic Input Patterns	1036
S. Mamagkakis, D. Soudris and F. Catthoor	
Lightweight Middleware for Seamless HW-SW Interoperability, with Application to Wireless Sensor Networks	1042
F.J. Villanueva, D. Villa, F. Moya, J. Barba, F. Rincón and J.C. López	

Interactive Presentation

A Middleware-Centric Design Flow for Networked Embedded Systems	1048
F. Fummi, G. Perbellini, R. Pietrangeli and D. Quaglia	

7.6: Advanced Architectures for Low Power Optimization

Moderators: J. Henkel, Karlsruhe U, DE; A. Macii, Politecnico di Torino, IT

Dynamic Reconfiguration in Sensor Networks with Regenerative Energy Sources.....	1054
A. Nahapetian, P. Lombardo, A. Acquaviva, L. Benini and M. Sarrafzadeh	
Dynamic Power Management under Uncertain Information	1060
H. Jung and M. Pedram	
Very Wide Register: An Asymmetric Register File Organization for Low Power Embedded Processors	1066
P. Raghavan, A. Lambrechts, M. Jayapala, F. Catthoor, D. Verkest and H. Corporaal	

Interactive Presentations

Single-Ended Coding Techniques for Off-Chip Interconnects to Commodity Memory	1072
M. Choudhury, K. Ringgenberg, S. Rixner and K. Mohanram	
PowerQuest: Trace Driven Data Mining for Power Optimization.....	1078
P. Babighian, G. Kamhi and M. Vardi	

7.7: Performance Analysis for NoC Architectures

Moderators: S. Murali, Stanford U, US; L. Carloni, UCB, ES

System Level Assessment of an Optical NoC in an MPSoC Platform	1084
M. Brière, B. Girodias, Y. Bouchebaba, G. Nicolescu, F. Mieyeville, F. Gaffiot and I. O'Connor	
Systematic Comparison between the Asynchronous and the Multi-Synchronous Implementations of a Network on Chip Architecture.....	1090
A. Sheibanyrad, I. Miro Panades and A. Greiner	
Analytical Router Modeling for Networks-on-Chip Performance Analysis	1096
U.Y. Ogras and R. Marculescu	

Interactive Presentation

Hard- and Software Modularity of the NOVA MPSoC Platform	1102
C. Sauer, M. Gries and S. Dirk	

8.1: TUTORIAL SESSION – State of the Art for Safety Critical Systems (Space and Aeronautics Special Day)

Organizers: S. Prudhomme, Airbus, FR; E. Lansard, Alcatel Alenia Space, FR

Moderator: S. Prudhomme, Airbus, FR

The Methodological and Technological Dimensions of Technology Transfer for Embedded Systems in Aeronautics and Space	1108
T. Pardessus, H. Daembkes, and R. Arning	

8.2: Secure Systems

Moderators: R. Pacalet, ENST, FR; R. Locatelli, STMicroelectronics, FR

Energy Evaluation of Software Implementations of Block Ciphers under Memory Constraints.....	1110
J. Großschädl, S. Tillich, C. Rechberger, M. Hofmann and M. Medwed	

An Area Optimized Reconfigurable Encryptor for AES-Rijndael.....	1116
M. Alam, S. Ray, D. Mukhopadhyay, S. Ghosh, D. RoyChowdhury and I. Sengupta	

Performance Aware Secure Code Partitioning.....	1122
S.H.K. Narayanan, M. Kandemir and R. Brooks	

Energy and Execution Time Analysis of a Software-Based Trusted Platform Module.....	1128
N. Aaraj, A. Raghunathan, S. Ravi and N.K. Jha	

8.3: Reliable Microarchitectures

Moderators: S. Vassiliadis, TU Delft, NL; P. Ienne, EPFL Lausanne, CH

Utilization of SECDED for Soft Error and Variation-Induced Defect Tolerance in Caches	1134
L.D. Hung, H. Irie, M. Goshima and S. Sakai	

Transient Fault Prediction Based on Anomalies in Processor Events.....	1140
S. Narayanasamy, A. Coskun and B. Calder	

Low-Cost Protection for SER Upsets and Silicon Defects	1146
M. Mehrara, M. Attariyan, S. Shyam, K. Constantinides, V. Bertacco and T. Austin	

Working with Process Variation Aware Caches	1152
M. Mutyam and V. Narayanan	

Interactive Presentations

An Enhanced Technique for the Automatic Generation of Effective Diagnosis-Oriented Test Programs for Processor	1158
E. Sánchez, M. Schillaci, G. Squillero and M. Sonza Reorda	

Functional and Timing Validation of Partially Bypassed Processor Pipelines	1164
Q. Zhu, A. Shrivastava and N. Dutt	

8.4: Formal Techniques to Enhance the Verification Flow

Moderators: V. Bertacco, U of Michigan, US; S. Quer, Politecnico di Torino, IT

A Compositional Approach to the Combination of Combinational and Sequential Equivalence Checking of Circuits without Known Reset States	1170
I.-H. Moon, B. Bjesse and C. Pixley	
Estimating Functional Coverage in Bounded Model Checking	1176
D. Große, U. Kühne and R. Drechsler	
Abstraction and Refinement Techniques in Automated Design Debugging.....	1182
S. Safarpour and A. Veneris	

Interactive Presentation

Automatic Hardware Synthesis from Specifications: A Case Study.....	1188
R. Bloem, S. Galler, B. Jobstmann, N. Piterman, A. Pnueli and M. Weiglhofer	

8.5: Interconnect Extraction and Synthesis

Moderators: R. Suaya, Mentor Graphics, FR; P. Feldmann, IBM T J Watson Research Center, US

pFFT in FastMaxwell: A Fast Impedance Extraction Solver for 3D Conductor Structures over Substrate.....	1194
T. Moselhy, X. Hu and L. Daniel	
Optimization-Based Wideband Basis Functions for Efficient Interconnect Extraction.....	1200
X. Hu, T. Moselhy, J. White and L. Daniel	
Thermally Robust Clocking Schemes for 3D Integrated Circuits	1206
M. Mondal, A.J. Ricketts, S. Kirolos, T. Ragheb, G. Link, N. Vijaykrishnan and Y. Massoud	
Double-Via-Driven Standard Cell Library Design	1212
T.-Y. Lin, T.-H. Lin, H.-H. Tung and R.-B. Lin	

Interactive Presentation

Analysis of Power Consumption and BER of Flip-flop Based Interconnect Pipelining	1218
J. Xu, A. Roy and M.H. Chowdhury	

8.6: EMBEDDED TUTORIAL/PANEL – A Future of Customizable Processors: Are We There Yet?

Organizers: L. Pozzi, Lugano U, CH; P. Paulin, STMicroelectronics, CA

Moderator: P. Paulin, STMicroelectronics, CA

A Future of Customizable Processors: Are We There Yet?	1224
L. Pozzi and P. G. Paulin	

8.7: Placement and Floorplanning

Moderators: J. Dielissen, NXP Semiconductors, NL; T. Shiple, Synopsys, FR

Fast and Accurate Routing Demand Estimation for Efficient Routability-Driven Placement	1226
P. Spindler and F.M. Johannes	
Yield-Aware Placement Optimization	1232
P. Azzoni, M. Bertoletti, N. Dragone, F. Fummi, C. Guardiani and W. Vendraminetto	
Microarchitecture Floorplanning for Sub-Threshold Leakage Reduction.....	1238
H. Mogal and K. Bazargan	

9.1.1: HOT TOPIC I – Industrial Applications (Space and Aeronautics Special Day)

Organizers: S. Prudhomme, Airbus, FR; E. Lansard, Alcatel Alenia Space, FR

Moderator: E. Lansard, Alcatel Alenia Space, FR

Industrial Applications	1244
X. Olive, J.-M. Pasquet and D. Flament	

9.1.2: LUNCH TIME KEYNOTE – Setting the Industrial Scene (Space and Aeronautics Special Day)

Organizers/Moderators: S. Prudhomme, Airbus, FR; E. Lansard, Alcatel Alenia Space, FR

Flying Embedded: The Industrial Scene and Challenges for Embedded Systems in Aeronautics and Space	1246
J. Botti	

9.2: Crypto Blocks and Security

Moderators: R. Locatelli, STMicroelectronics, IT; R. Pacalet, ENST, FR

Compact Hardware Design of Whirlpool Hashing Core.....	1247
T. Alho, P. Hämmäläinen, M. Hämmäläinen and T.D. Hämmäläinen	

An Efficient Polynomial Multiplier in $GF(2^m)$ and Its Application to ECC Designs.....	1253
S. Peter and P. Langendörfer	

Flexible Hardware Reduction for Elliptic Curve Cryptography in $GF(2^m)$	1259
S. Peter, P. Langendörfer and K. Piotrowski	

Overcoming Glitches and Dissipation Timing Skews in Design of DPA-Resistant Cryptographic Hardware.....	1265
K.J. Lin, S.C. Fang, S.-H. Yang, and C.C. Lo	

9.3: Variation Tolerant Mixed Signal Test

Moderators: A. Rubio, UP Catalunya, ES; S. Mir, TIMA Laboratory, FR

Dynamic Critical Resistance: A Timing-Based Critical Resistance Model for Statistical Delay Testing of Nanometer ICs.....	1271
J.L. Rosselló, C. de Benito, S.A. Bota, J. Segura	

Sensitivity Analysis for Fault-Analysis and Tolerance in RF Front-End Circuitry	1277
T. Das and P.R. Mukund	

A Two-Tone Test Method for Continuous-Time Adaptive Equalizers.....	1283
D. Hong, S. Saberi, K.-T. Cheng and C.P. Yue	

Worst-Case Design and Margin for Embedded SRAM	1289
R. Aitken and S. Idgunji	

Interactive Presentations

Pulse Propagation for the Detection of Small Delay Defects.....	1295
M. Favalli and C. Metra	

BIST Method for Die-Level Process Parameter Variation Monitoring in Analog/Mixed-Signal Integrated Circuits.....	1301
A. Zjajo, M.J. Barragan Asian and J. Pineda de Gyvez	

9.4: SAT Techniques for Verification

Moderators: R. Bloem, TU Graz, AT; R. Drechsler, Bremen U, DE

A New Hybrid Solution to Boost SAT Solver Performance.....	1307
L. Fang and M.S. Hsiao	
QuteSAT: A Robust Circuit-Based SAT Solver for Complex Circuit Structure	1313
C.-A. Wu, T.-H. Lin, C.-C. Lee and C.-Y. Huang	
Boosting the Role of Inductive Invariants in Model Checking.....	1319
G. Cabodi, S. Nocco and S. Quer	

Interactive Presentation

Image Computation and Predicate Refinement for RTL Verilog Using Word Level Proofs.....	1325
D. Kroening and N. Sharygina	

9.5: Compiler Techniques for Customisable Architectures

Moderators: A. Darte, ENS Lyon, FR; H. van Someren, ACE Associated Compiler Experts, NL

Polynomial-Time Subgraph Enumeration for Automated Instruction Set Extension	1331
P. Bonzini and L. Pozzi	
Interrupt and Low-Level Programming Support for Expanding the Application Domain of Statically-Scheduled Horizontally-Microcoded Architectures in Embedded Systems	1337
M. Reshadi and D. Gajski	
DRIM: A Low Power Dynamically Reconfigurable Instruction Memory Hierarchy for Embedded Systems	1343
Z. Ge, W.-F. Wong and H.-B. Lim	

Interactive Presentations

SoftSIMD – Exploiting Subword Parallelism Using Source Code Transformations.....	1349
S. Kraemer, R. Leupers, G. Ascheid and H. Meyr	
A Process Splitting Transformation for Kahn Process Networks	1355
S. Meijer, B. Kienhuis, A. Turjan and E. de Kock	

9.6: Interconnect Optimization and Metastability

Moderators: S. Sapatnekar, Minnesota U, US; T. Shiple, Synopsys, FR

Computing Synchronizer Failure Probabilities	1361
S. Yang and M. Greenstreet	
Layout-Aware Gate Duplication and Buffer Insertion.....	1367
D. Bañeres, J. Cortadella and M. Kishinevsky	
Self-Heating-Aware Optimal Wire Sizing under Elmore Delay Model.....	1373
M. Ni and S.O. Memik	

9.7: Physical and Device Simulation

Moderators: M. Zwolinski, Southampton U, UK; F. Gaffiot, Ecole Centrale de Lyon, FR

Statistical Blockade: A Novel Method for Very Fast Monte Carlo Simulation of Rare Circuit Events, and Its Application	1379
A. Singhee and R.A. Rutenbar	

Clock Domain Crossing Fault Model and Coverage Metric for Validation of SoC Design	1385
Y. Feng, Z. Zhou, D. Tong and X. Cheng	

Fast Statistical Circuit Analysis with Finite-Point Based Transistor Model	1391
M. Chen, W. Zhao, F. Liu and Y Cao	

Interactive Presentation

Statistical Simulation of High-Frequency Bipolar Circuits.....	1397
W. Schneider, M. Schroter, W. Kraus and H. Wittkopf	

10.1: HOT TOPIC II – Development and Industrialization (Space and Aeronautics Special Day)

Organizers/Moderators: S. Prudhomme, Airbus, FR; E. Lansard, Alcatel Alenia Space, FR

Development and Industrialization	1403
M. Riffiod, P. Caspi, C. Piala and J.-L. Voirin	

10.2: Wireless Communication and Networking System Implementation

Moderators: C. Heer, Infineon Technologies, DE ; O. Deprez, Texas Instruments, FR

Low Power Design on Algorithmic and Architectural Level: A Case Study of an HSDPA Baseband Digital Signal Processing System	1406
M. Schämamm, S. Hessel, U. Langmann and M. Bücken	

Mapping the Physical Layer of Radio Standards to Multiprocessor Architectures.....	1412
C. Grassmann, M. Richter and M. Sauermann	

Development of an ASIP Enabling Flows in Ethernet Access Using a Retargetable Compilation Flow	1418
K. Van Renterghem, P. Demuytere, D. Verhulst, J. Vandewege and X.-Z. Qiu	

An Effective AMS Top-Down Methodology Applied to the Design of a Mixed-Signal UWB System-on-Chip	1424
M. Crepaldi, M.R. Casu, M. Graziano and M. Zamboni	

Interactive Presentation

Behavioral Modeling of Delay-Locked Loops and Its Application to Jitter Optimization in Ultra Wide-Band Impulse Radio Systems	1430
E. Barajas, R. Cosculluela, D. Coutinho, D. Mateo, J. L. González, I. Cairò, S. Banda, M. Ikeda	

10.3: Soft Error Evaluation and Tolerance

Moderators: C. Metra, Bologna U, IT; B. Gottlieb, Intel, US

Soft Error Rate Analysis for Sequential Circuits	1436
N. Miskov-Zivanov and D. Marculescu	

Verification-Guided Soft Error Resilience.....	1442
S.A. Seshia, W. Li and S. Mitra	

A Low-SER Efficient Core Processor Architecture for Future Technologies 1448
E.L. Rhod, C.A. Lisbôa and L. Carro

Accurate and Scalable Reliability Analysis of Logic Circuits 1454
M.R. Choudhury and K. Mohanram

Interactive Presentation

A New Asymmetric SRAM Cell to Reduce Soft Errors and Leakage Power in FPGA..... 1460
B.S. Gill, C. Papachristou and F.G. Wolff

10.4: EMBEDDED TUTORIAL – EDA – A Pivotal Theme in the European Technology Platforms - ARTEMIS and ENIAC

Organizers/Moderators: P. Magarshack, STMicroelectronics, FR; E. Schutz, STMicroelectronics, BE

Design Challenges at 65nm and Beyond..... 1466
A.B. Kahng

The ARTEMIS Cross-Domain Architecture for Embedded Systems 1468
H. Kopetz

HW/SW Implementation from Abstract Architecture Models..... 1470
A.A. Jerraya

10.5: Memory and Instruction-Set Customization for Real-Time Systems

Moderators: T.-W. Kuo, National Taiwan U, ROC ; H. van Someren, ACE Associated Compiler Experts, NL

Instruction-Set Customization for Real-Time Embedded Systems..... 1472
H.P. Huynh and T. Mitra

A Novel Technique to Use Scratch-Pad Memory for Stack Management 1478
S. Park, H.-W. Park and S. Ha

Scratchpad Memories vs Locked Caches in Hard Real-Time Systems: A Quantitative Comparison 1484
I. Puaut and C. Pais

Task Scheduling for Reliable Cache Architectures of Multiprocessor Systems 1490
M. Sugihara, T. Ishihara and K. Murakami

10.6: Order Reduction and Variation-Aware Interconnect Modelling

Moderators: L. Daniel, Massachusetts Institute of Technology, US; L.M. Silveira, TU Lisbon, PT

Fast Positive-Real Balanced Truncation of Symmetric Systems Using Cross Riccati Equations..... 1496
N. Wong

Random Sampling of Moment Graph: A Stochastic Krylov-Reduction Algorithm 1502
Z. Zhu and J. Phillips

Statistical Model Order Reduction for Interconnect Circuits Considering Spatial Correlations..... 1508
J. Fan, N. Mi, S.X.-D. Tan, Y. Cai and X. Hong

A Sparse Grid Based Spectral Stochastic Collocation Method for Variations-Aware Capacitance Extraction of Interconnects under Nanometer Process Technology 1514
H. Zhu, X. Zeng, W. Cai, J. Xue and D. Zhou

Interactive Presentation

Simulation Methodology and Experimental Verification for the Analysis of Substrate Noise on LC-VCO's..... 1520
S. Bronckers, C. Soens, G. Van Der Plas, G. Vandersteen and Y. Rolain

10.7: Temperature and Process Aware Low Power Techniques

Moderators: C. Silvano, Politecnico di Milano, IT; E. Schmidt, ChipVision Design Systems, DE

Accurate Temperature-Dependent Integrated Circuit Leakage Power Estimation Is Easy..... 1526
Y. Liu, R.P. Dick, L. Shang and H. Yang

Low-Overhead Circuit Synthesis for Temperature Adaptation Using Dynamic Voltage Scheduling 1532
S. Ghosh, S. Bhunia and K. Roy

Maximum Circuit Activity Estimation Using Pseudo-Boolean Satisfiability 1538
H. Mangassarian, A. Veneris, S. Safarpour, F.N. Najm and M.S. Abadir

Interactive Presentations

Efficient Computation of Discharge Current Upper Bounds for Clustered Sleep Transistor Sizing 1544
A. Sathanur, A. Calimera, L. Benini, A. Macii, E. Macii and M. Poncino

Process Tolerant Beta-Ratio Modulation for Ultra-Dynamic Voltage Scaling..... 1550
M.-E. Hwang, T. Cakici and K. Roy

11.1: PANEL SESSION – Towards Total Open Source in Aeronautics and Space? (Space and Aeronautics Special Day)

Organizers: S. Prudhomme, Airbus, FR; E. Lansard, Alcatel Alenia Space, FR

Moderator: P. Aycinena, Editor, EDA Confidential, US

Towards Total Open Source in Aeronautics and Space? 1556
Panelists: E. Bantegnie, G. Ladier, R. Mueller, F. Gasperoni and A. Wilson

11.2: Wireless Communication and Networking Algorithms

Moderators: C. Grassmann, Infineon Technologies, DE ; O. Deprez, Texas Instruments, FR

A Tiny and Efficient Wireless Ad-Hoc Protocol for Low-Cost Sensor Networks 1557
P. Gburzynski, B. Kaminska and W. Olesinski

Scalable Reconfigurable Channel Decoder Architecture for Future Wireless Handsets..... 1563
G. Krishnaiah, N. Engin and S. Sawitzki

A New Pipelined Implementation for Minimum Norm Sorting Used in Square Root
Algorithm for MIMO-VBLAST Systems 1569
Z. Khan, T. Arslan, J.S. Thompson, A.T. Erdogan

Optimization of the 'FOCUS' Inband-FEC Architecture for 10-Gbps SDH/SONET Optical
Communication Channels 1575
A. Tychopoulos and O. Koufopavlou

11.3: System Reliability and Security Issues

Moderators: C. Bolchini, Politecnico di Milano, IT; S. Bocchio, STMicroelectronics, IT

A Framework for System Reliability Analysis Considering Both System Error Tolerance and Component Test Quality	1581
S.-J. Pan and K.-T. Cheng	
Experimental Evaluation of Protections against Laser-Induced Faults and Consequences on Fault Modeling.....	1587
R. Leveugle, A. Ammari, V. Maingot, E. Teyssou, P. Moitrel, C. Mourtel, N. Feyt, J.-B. Rigaud and A. Tria	
Evaluation of Design for Reliability Techniques in Embedded Flash Memories	1593
B. Godard, J.-M. Daga, L. Torres and G. Sassatelli	
Reduction of Detected Acceptable Faults for Yield Improvement via Error-Tolerance	1599
T.-Y. Hsieh, K.-J. Lee and M.A. Breuer	

11.4: Statistical Timing and Worst-Delay Corner Analysis

Moderators: M. Berkelaar, Magma Design Automation, NL; J. Cortadella, UP Catalunya, ES

Use of Statistical Timing Analysis on Real Designs.....	1605
A. Nardi, E. Tuncer, S. Naidu, A. Antonau, S. Gradinaru, T. Lin and J. Song	
A Novel Criticality Computation Method in Statistical Timing Analysis	1611
F. Wang, Y. Xie and H. Ju	
Efficient Computation of the Worst-Delay Corner	1617
L. Guerra e Silva, L.M. Silveira and J.R. Phillips	

11.5: Real-Time Methodologies

Moderators: I. Puaut, Rennes U/IRISA, FR; S. Baruah, North Carolina U, US

Accounting for Cache-Related Preemption Delay in Dynamic Priority Schedulability Analysis.....	1623
L. Ju , S. Chakraborty and A. Roychoudhury	
Energy-Efficient Real-Time Task Scheduling with Task Rejection	1629
J.-J. Chen, T.-W. Kuo, C.-L. Yang and K.-J. King	
Feasibility Intervals for Multiprocessor Fixed-Priority Scheduling of Arbitrary Deadline Periodic Systems.....	1635
L. Cucu and J. Goossens	
Energy Minimization with Soft Real-Time and DVS for Uniprocessor and Multiprocessor Embedded Systems	1641
M. Qiu, C. Xue, Z. Shao and E.H.-M. Sha	

11.6: Impact of Nanometer Technologies in MPSoCs and SoC Design

Moderators: R. Marculescu, Carnegie Mellon U, US; D. Atienza, DACYA – Madrid Complutense U, ES

Joint Consideration of Fault-Tolerance, Energy-Efficiency and Performance in On-Chip Networks	1647
A. Ejlali, B.M. Al-Hashimi, P. Rosinger and S.G. Miremadi	
Impact of Process Variations on Multicore Performance Symmetry	1653
E. Humenay, D. Tarjan and K. Skadron	

Temperature Aware Task Scheduling in MPSoCs.....	1659
A. Kivilcim Coskun, T. Simunic Rosing and K. Whisnant	

11.7: High-Level Memory and Clock Power Optimization

Moderators: R. Zafalon, STMicroelectronics, IT; J. Haid, Infineon Technologies, DE

Architectural Leakage-Aware Management of Partitioned Scratchpad Memories.....	1665
O. Golubeva, M. Loghi, M. Poncino and E. Macii	

Memory Bank Aware Dynamic Loop Scheduling.....	1671
M. Kandemir, T. Yemliha, S.W. Son and O. Ozturk	

System Level Clock Tree Synthesis for Power Optimization.....	1677
S.A. Butt, S. Schermbeck, J. Rosenthal, A. Pratsch and E. Schmidt	

Author Index	A-1
---------------------------	-----