PROCEEDINGS OF SPIE

Design-Process-Technology Co-optimization for Manufacturability XII

Jason P. Cain
Chi-Min Yuan
Editors

28 February–1 March 2018
San Jose, California, United States

Sponsored by
SPIE

Cosponsored by
Hitachi High Technologies, America, Inc. (United States)

Published by
SPIE

Volume 10588

Proceedings of SPIE 0277-786X, V. 10588

SPIE is an international society advancing an interdisciplinary approach to the science and application of light.

The papers in this volume were part of the technical conference cited on the cover and title page. Papers were selected and subject to review by the editors and conference program committee. Some conference presentations may not be available for publication. Additional papers and presentation recordings may be available online in the SPIE Digital Library at SPIEDigitalLibrary.org.

The papers reflect the work and thoughts of the authors and are published herein as submitted. The publisher is not responsible for the validity of the information or for any outcomes resulting from reliance thereon.

Please use the following format to cite material from these proceedings:
Author(s), "Title of Paper," in *Design-Process-Technology Co-optimization for Manufacturability XII*, edited by Jason P. Cain, Chi-Min Yuan, Proceedings of SPIE Vol. 10588 (SPIE, Bellingham, WA, 2018) Seven-digit Article CID Number.

ISSN: 0277-786X
ISSN: 1996-756X (electronic)

ISBN: 9781510616684
ISBN: 9781510616691 (electronic)

Published by
SPIE
P.O. Box 10, Bellingham, Washington 98227-0010 USA
Telephone +1 360 676 3290 (Pacific Time)· Fax +1 360 647 1445
SPIE.org
Copyright © 2018, Society of Photo-Optical Instrumentation Engineers.

Copying of material in this book for internal or personal use, or for the internal or personal use of specific clients, beyond the fair use provisions granted by the U.S. Copyright Law is authorized by SPIE subject to payment of copying fees. The Transactional Reporting Service base fee for this volume is $18.00 per article (or portion thereof), which should be paid directly to the Copyright Clearance Center (CCC), 222 Rosewood Drive, Danvers, MA 01923. Payment may also be made electronically through CCC Online at copyright.com. Other copying for republication, resale, advertising or promotion, or any form of systematic or multiple reproduction of any material in this book is prohibited except with permission in writing from the publisher. The CCC fee code is 0277-786X/18/$18.00.

Printed in the United States of America Vm7 i ffUb 5ggcWJUhYgž bWži bXYf`]WYbgY Zfca GD=9.

Publication of record for individual papers is online in the SPIE Digital Library.

SPIE. DIGITAL LIBRARY
SPIEDigitalLibrary.org

Paper Numbering: *Proceedings of SPIE* follow an e-First publication model. A unique citation identifier (CID) number is assigned to each article at the time of publication. Utilization of CIDs allows articles to be fully citable as soon as they are published online, and connects the same identifier to all online and print versions of the publication. SPIE uses a seven-digit CID article numbering system structured as follows:

- The first five digits correspond to the SPIE volume number.
- The last two digits indicate publication order within the volume using a Base 36 numbering system employing both numerals and letters. These two-number sets start with 00, 01, 02, 03, 04, 05, 06, 07, 08, 09, 0A, 0B … 0Z, followed by 10-1Z, 20-2Z, etc. The CID Number appears on each page of the manuscript.

Contents

vii *Authors*
ix *Conference Committee*

SESSION 1 TRENDS IN DPTCO

10588 03 **Efficient place and route enablement of 5-tracks standard-cells through EUV compatible N5 ruleset** [10588-2]

10588 04 **Patterning method impact on sub-36nm pitch interconnect variability** [10588-3]

10588 05 **Applying machine learning to pattern analysis for automated in-design layout optimization** [10588-4]

SESSION 2 PATTERN CORRECTION METHODS: JOINT SESSION WITH CONFERENCES 10588 AND 10587

10588 06 **Optimization of optical proximity correction to reduce mask write time using genetic algorithm** [10588-5]

10588 07 **Dependencies of bias tables to pattern density, critical dimension, global coordinates and pattern orientation for nanoimprint master manufacturing for the 200 mm wafer scale SmartNIL process** [10588-6]

SESSION 3 DESIGN-TECHNOLOGY CO-OPTIMIZATION

10588 08 **Pre-PDK block-level PPAC assessment of technology options for sub-7nm high-performance logic (Invited Paper)** [10588-7]

10588 09 **Track height reduction for standard-cell in below 5nm node: how low can you go?** [10588-8]

10588 0A **A compact multi-bit flip-flop with smaller height implementation and metal-less intra-cell routing** [10588-9]

10588 0B **DTCO exploration for efficient standard cell power rails** [10588-10]

SESSION 4 LAYOUT OPTIMIZATION

10588 0C **Post-decomposition optimizations using pattern matching and rule-based clustering for multi-patterning technology** [10588-11]

10588 0D **Pin routability and pin access analysis on standard cells for layout optimization** [10588-12]

10588 0E **Variability-aware double-patterning layout optimization for analog circuits** [10588-13]

10588 0F **Litho friendly via insertion with in-design auto-fix flow using machine learning** [10588-14]

SESSION 5 DESIGN INTERACTIONS: JOINT SESSION WITH CONFERENCES 10585 AND 10588

10588 0G **A model-based, Bayesian approach to the CF_4/Ar etch of SiO_2** [10588-15]

SESSION 6 PATTERN-BASED ANALYSIS

10588 0J **Range pattern matching with layer operations and continuous refinements** [10588-19]

10588 0K **Combinational optical rule check on hotspot detection** [10588-20]

10588 0L **Pattern analysis and classification accelerates OPC tuning, monitoring, and optimization and mask inspection** [10588-21]

SESSION 7 ADVANCED PATTERNING

10588 0N **IMEC N7, N5 and beyond: DTCO, STCO and EUV insertion strategy to maintain affordable scaling trend (Invited Paper)** [10588-22]

10588 0O **Relaxing LER requirement in EUV lithography** [10588-23]

10588 0P **Comparison between multi-colored LE^n SADP/SAQP and selective-etching SADP/SAQP** [10588-25]

10588 0Q **Integrated manufacturing flow for selective-etching SADP/SAQP** [10588-24]

POSTER SESSION

10588 0R **Timing optimization in SADP process through wire widening and double via insertion** [10588-26]

10588 0S **Characterization of metal line-width variation in via first dual-damascene approach and its modeling using machine learning artificial neural network algorithms** [10588-27]

10588 0T **Cross-MEEF assisted SRAF print avoidance approach** [10588-28]

10588 0U **A weak pattern random creation and scoring method for lithography process tuning** [10588-29]

10588 0V **Pattern-based IP block detection, verification, and variability analysis** [10588-30]

10588 0W **A smart way to identify and extract repeated patterns of a layout** [10588-31]

10588 0X **Using pattern based layout comparison for a quick analysis of design changes** [10588-32]

10588 0Y **An efficient way of layout processing based on calibre DRC and pattern matching for defects inspection application** [10588-33]

10588 0Z **Leveraging pattern matching to solve SRAM verification challenges at advanced nodes** [10588-34]

10588 10 **A portable pattern-based design technology co-optimization flow to reduce optical proximity correction run-time** [10588-35]

10588 11 **Hybrid hotspot library building based on optical and geometry analysis at early stage for new node development** [10588-36]